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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,805	02/27/2004	Reidar Lindstedt	2002 P 16328 US	7850
48154	7590	02/24/2006	EXAMINER	
SLATER & MATSIL LLP 17950 PRESTON ROAD SUITE 1000 DALLAS, TX 75252				VU, HUNG K
		ART UNIT		PAPER NUMBER
		2811		

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/788,805	LINDSTEDT, REIDAR
	Examiner	Art Unit
	Hung Vu	2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 09 December 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-7,9-13 and 20-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-7,9-13 and 20-27 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____. |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____. | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____. |

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Malba (PN 5,834,162).

Malba discloses, as shown in Figures 1-3, a semiconductor chip arrangement comprising:

a mount element (substrate, not shown, Col. 4, lines 28-41 or bottom 10);

a first semiconductor substrate (bottom 10 or middle 10) including at least one interconnect (14) formed on the first semiconductor substrate and also including at least one contact area (17) that is electrically connected to the interconnect and is arranged on a side surface of the first semiconductor substrate; and

a second semiconductor substrate (middle 10 or top 10) having at least one interconnect (14) formed on the second semiconductor substrate and also including at least one contact area (17) that is electrically connected to the interconnect and is arranged on a side surface of the second semiconductor substrate;

wherein the second semiconductor substrate is arranged on the first semiconductor substrate and the first semiconductor substrate is arranged on the mount element such that a first main surface of the second semiconductor substrate rests on the first semiconductor substrate,

and a first main surface of the first semiconductor substrate rests on the mount element, and wherein an electrical contact is produced between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate and wherein the first and second semiconductor substrates each comprise an unpackaged semiconductor chip with integrated circuitry disposed therein.

Regarding claim 2, Malba discloses the first and second semiconductor substrates each have an integrated circuit disposed in the area of the first main surface, wherein, for both the first and second semiconductor substrates, the integrated circuit is electrically coupled to the interconnect.

Regarding claim 3, Malba discloses the semiconductor chip arrangement further comprising a conductive material (13) applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

Regarding claim 4, Malba discloses the first main surface of the first semiconductor substrate is attached to the mount element.

Regarding claim 25, Malba discloses the second semiconductor substrate is arranged in direct contact with the first semiconductor substrate and the first semiconductor substrate is arranged in direct contact with the mount element.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5-7, 9-13, 20-25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malba (PN 5,834,162) in view of Glenn (PN 6,518,659, of record).

Regarding claim 7, Malba discloses, as shown in Figures 1-3, a semiconductor chip arrangement comprising:

a second semiconductor substrate (bottom 10) arranged over the mount element alongside the first semiconductor substrate, the second semiconductor substrate including at least one interconnect (14) formed thereon, the second semiconductor substrate further including at least one contact area (17) that is electrically connected to the interconnect and is arranged along a side surface of the second semiconductor substrate; and

a third semiconductor substrate (middle 10) arranged over the second semiconductor substrate, the third semiconductor substrate including at least one interconnect (14) formed thereon, the third semiconductor substrate further including at least one contact area (17) that is electrically connected to the interconnect and is arranged along a side surface of the third semiconductor substrate, the third semiconductor substrate arranged so that an electrical contact is produced between the contact area of the third semiconductor substrate and the contact area of the second semiconductor substrate.

Malba further discloses the chips can stack on each other to form the chips stacked and that other chips (the first semiconductor substrate) having the similar structure can be formed adjacent the chips stacked due to the sidewall bond pads (17). Col. 4, lines 18-27. Malba does not clearly show the second semiconductor substrate arranged so that an electrical contact is produced between the contact area of the first semiconductor substrate and the contact area of the second semiconductor substrate and the first, second and third semiconductor substrates forms on a mount element. However, Glenn disclose a mount element (not shown, 31) having the first, second, and third semiconductor substrates (44,44,44) form thereon and the second semiconductor substrate arranged so that an electrical contact is produced between the contact area of the first semiconductor substrate and the contact area of the second semiconductor substrate. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the structure of Malba having the first, second, and third semiconductor substrates form on the mount element, and the second semiconductor substrate arranged so that an electrical contact is produced between the contact area of the first semiconductor substrate and the contact area of the second semiconductor substrate, such as taught by Glenn in order to easily add more semiconductor substrate/chip to increase the circuit density without increasing the mounting area on a printed circuit board.

Regarding claim 9, Malba and Glen disclose the semiconductor chip arrangement further comprising a conductive material (14) applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

Regarding claim 10, Malba and Glen disclose the first semiconductor substrate is attached to the mount element and wherein the second semiconductor substrate is attached to the mount element.

Regarding claims 5, 11 and 24, Malba and Glen disclose the contact areas on the first and the second semiconductor substrates each extend from a first main surface to a second main surface of the respective semiconductor substrate.

Regarding claim 12, Malba and Glen disclose the contact area on the third semiconductor substrate extends to a first main surface on the third semiconductor substrate.

Regarding claims 6, 13 and 25, Malba and Glen disclose each of the first, second, and third semiconductor substrates includes a dynamic random access memory formed therein.

Regarding claim 21, Malba and Glen disclose each of the integrated circuitry is electrically coupled to the interconnect.

Regarding claim 22, Malba and Glen disclose the semiconductor chip arrangement further comprising a conductive material (14) applied between the contact area on the first semiconductor substrate and the contact area on the second semiconductor substrate.

Regarding claim 23, Malba and Glen disclose the first semiconductor substrate is attached to the mount element and wherein the second semiconductor substrate is attached to the mount element.

Regarding claim 27, Malba and Glen disclose the first semiconductor substrate is arranged in direct contact with the surface of the mount element, the second semiconductor substrate arranged in direct contact with the surface of the mount element, and the third semiconductor substrate is arranged in direct contact with the second semiconductor substrate.

Response to Arguments

3. Applicant's arguments with respect to claims 1 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung Vu whose telephone number is (571) 272-1666. The examiner can normally be reached on Tuesday to Friday 6:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272 - 1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vu

February 15, 2006

Hung Vu

Hung Vu

Primary Examiner